REMARKS

Claims 1-20 were previously pending. Reconsideration of presently pending claims 1-20 is respectfully requested in light of the above amendments and the following remarks.

Allowable Subject Matter

Noted with appreciation is the indication that claims 10 and 17 are directed at allowable subject matter and would be allowed if rewritten in independent form. However, claims 10 and 17 depend from rejected base claims but, for reasons set forth below, it is believed that the rejected claims are allowable. Accordingly, it is believed unnecessary to separately place claims 10 and 17 in independent form at this time.

Rejections under 35 U.S.C. §102

Claim 1 recites:

> A method for accessing a plurality of memory compiler units, the method comprising:
> prompting, via a multi-compiler interface, for a selection of a first memory compiler unit from a plurality of memory compiler units;
> remotely linking to the selected first memory compiler unit; and
> generating a combination datasheet comprising a plurality of memory instances.

Claim 1 stands rejected under 35 U.S.C. §102(e) as being anticipated by Dangelo et al. (U.S. Patent No. 5,493,508 hereinafter referred to as "Dangelo"). The PTO specifies in MPEP §2131 that, in order for a reference to anticipate a claim under §102, the reference must teach each and every element recited in the claim. Therefore, to maintain this rejection with respect to claim 1, the Dangelo reference must contain all of the above-claimed elements of the claim. However, Dangelo does not teach a method for accessing a plurality of memory compiler units including the feature of "prompting, via a multi-compiler interface, for a selection of a first memory compiler unit from a plurality of memory compiler units."

More specifically, the Examiner indicated that this feature is allegedly disclosed by Dangelo in Col. 10, lines 50-60. The cited passage of Dangelo recites the following:

> ... description in the optimization environment can be beneficial for optimization of the chip's core part.

> The exemplary chip 110 includes the following major functional blocks: memory 112, data path 114, mega-cells and mega-functions 116 and functional units 118 which may include regular blocks 120 such as adders and decoders and random logic 122.
>
> The memory block 112 is generated by memory compilers using efficient technology-dependent building blocks. The output of the memory complier is a net list of primitive transistors.

From the above, Dangelo generally describes the major functional blocks of a chip design including a memory block generated by memory compilers. As such, Dangelo discloses a methodology for generating structural descriptions of complex digital devices from high-level descriptions and specifications. (See Dangelo, Abstract). No where in the cited passage does it teach "prompting, via a multi-compiler interface, for a selection of a first memory compiler unit from a plurality of compiler units," as is recited in claim 1. The Examiner further alleges that, "generating the memory blocks as pointed out above [] include[s] the use of more than one memory compiler." Applicants respectfully disagree. The Dangelo reference shows one memory compiler unit (reference number 602) in Figures 6 and 8 and specifies that, "A Memory Compiler (MemComp) 602 takes the high level specification for memory mega-cells and produces logic and layout files for the purpose of simulating, testing and layout." (See Dangelo, Col. 13, lines 62-65). Here, the feature of prompting for a selection of a first memory compiler unit from a plurality of memory compiler units is via a multi-compiler interface.

As another example, the Dangelo reference does not teach a method for accessing a plurality of memory compiler units including the feature of "remotely linking to the selected first memory compiler unit." More specifically, the Examiner indicated that this feature is allegedly disclosed by Dangelo in Col. 18, lines 1-5. The cited passage of Dangelo recites the following:

> [Illustrative tools (ChipSizer, MemComp, LCMP, LLINK, LVER, LDEL, LCAP, LSIM, LBOND and LPACE), com]merically available within LSI Logic's Modular Design Environment 830 are shown. Generally, these tools consist of a set of programs that compile, link, simulate and verify digital logic at the chip (structural) level. Any number of other, commercially available programs could be employed at this level to perform similar functions.

Figure 8 of Dangelo, as shown below, illustrates the Modular Design Environment (reference number 830) including the MemComp as well as the other tools.

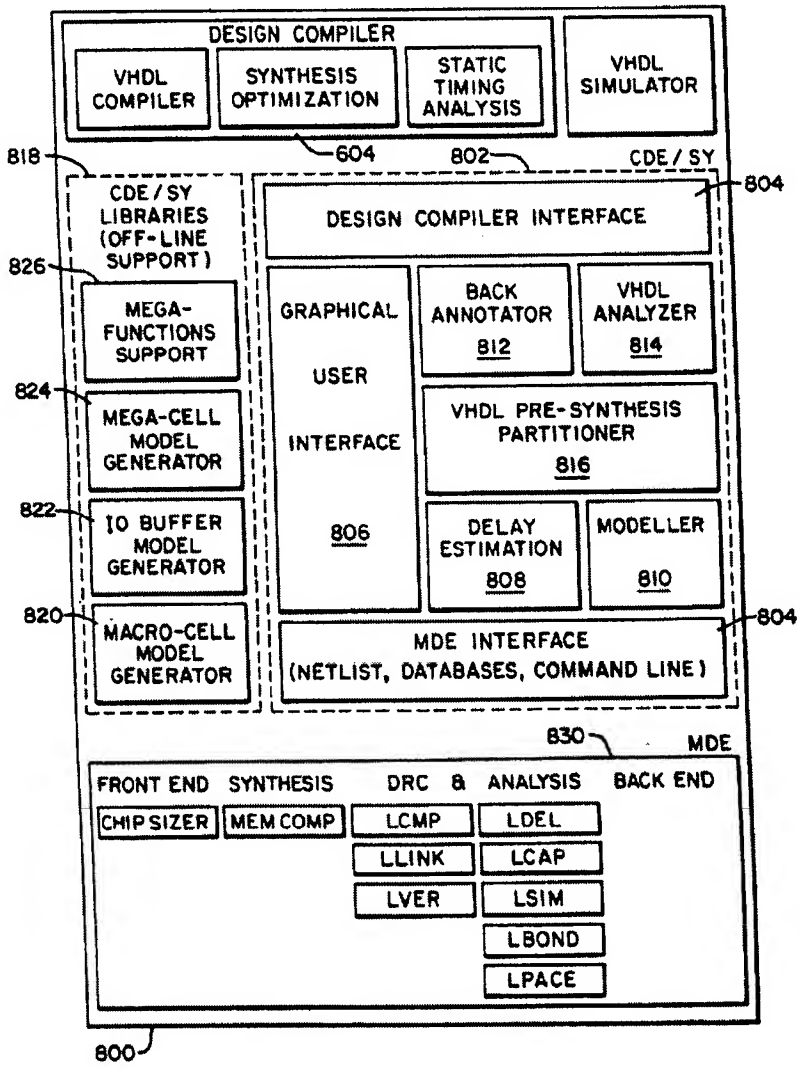

FIG. 8

From the above, it is clear that the cited passage of Dangelo does not teach "remotely linking to the selected first memory compiler unit," as is recited in claim 1. Instead, Dangelo teaches that the tools such as MemComp, LLINK, LSIM, and LVER in the Modular Design Environment consist of programs that compile, link, simulate and verify digital logic at the chip level. Here, claim 1 recites "remotely linking to the first selected memory compiler unit" after it has been selected from a plurality of memory compiler units. As indicated in the present application, it is

desired to provide memory compilers that can be accessed through a single platform from anywhere and anytime. (See Present Application, par. [0026]).

Accordingly, the rejection under 35 U.S.C. §102 with respect to claim 1 is not supported by the Dangelo reference and therefore, should be withdrawn.

Claims 13 and 19 stand rejected under 35 U.S.C. §102(e) as being anticipated by Dangelo under essentially the same rationale in which claim 1 was rejected. Claims 13 and 19 are allowable for at least the same reasons as set forth above for claim 1. Additionally, claims 13 and 19 recite in part, a combination datasheet comprising a plurality of memory instances created by different memory compiler units. The Examiner alleges that this feature is disclosed by Dangelo in Col. 14, lines 8-15. The cited passage of Dangelo recites the following:

> ... 1) (not shown) the data sheet generated by MemComp is used to manually extract the timing description of the memory block. This basically involves defining a set of "set_load", "set_drive" and "set_arrival" constraints and associating them with the relevant pins of the surrounding logic at the start of the optimization process; or 2) a Memory Modeler (see FIG. 8) is used to generate a model 603 in Synopsys Library Language (SLL; available from LSI Logic Corporation).

From the above, it is clear that Dangelo teaches that the data sheet is generated by MemComp, a single and same memory compiler unit. In addition, the Memory Modeler is used to generate a model from the memory description and thus, is not equivalent to a memory compiler unit. Here, the combination datasheet is generated with a plurality of memory instances created by different memory compiler units.

Accordingly, the rejection under 35 U.S.C. §102 with respect to claims 13 and 19 is not supported by the Dangelo reference, and therefore, should be withdrawn.

Conclusion

It is clear from all of the foregoing that independent claims 1, 13, and 19 are in condition for allowance. Claims 2-12, 14-18, and 20 depend from, either directly or indirectly, and further limit independent claims 1, 13, and 19 and therefore are allowable as well.

A timely issuance of a Notice of Allowance for claims 1-20 is respectfully requested. The Examiner is invited to call the undersigned at the below-listed number if a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

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Dated: 6-1-07

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I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on June 1, 2007.

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